**Introduction**

The purpose of this lab was to design a sequential circuit using synthesis techniques. We had to design a sequential circuit to detect the input sequence “1010”. A tutorial was given to do just that with the exception of recognizing overlaps. For the lab, we had to include overlaps.

**Preliminary Work**

Design the sequential circuit to detect the sequence.

**state diagram**



The next step in the design process is to develop a state table from the state diagram.

**state table**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Q1** | **Q0** | **X** | **D1** | **D0** | **Z** |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 1 | 0 |

Once the state table has been defined, K-maps were used to obtain the equations that describe the relationship between the inputs and outputs of the circuit.

**K-Maps**



**Lab Work**

Then the equations are translated into VHDL and a stimulus is created.

**VHDL**

--equations

D1<=(Q0 and (not X)) OR (Q1 and (not Q0) and X);

D0<=X;

Z <=Q1 and Q0 and (not X);

--stimulus

x <= '0', '1' after 20ns, '0' after 40ns, '1' after 60ns, '0' after 80ns,

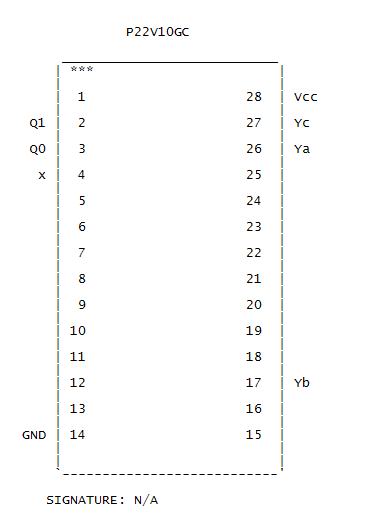
'1' after 100ns, '0' after 120ns, '1' after 140ns;

Q0 <= '0', '1' after 40ns, '0' after 80ns, '1' after 120ns;

Q1 <= '0', '1' after 80ns;

After running a test bench and synthesis, the JED file is obtained along with a diagram of the GAL chip and its associated inputs.

**GAL Chip**



Combining the GAL diagram inputs/outputs and the following given diagram gives the full circuit diagram. Note that the 7474 chip contains two flip flips within it.

**Circuit Diagram**



The wire list was simple because no logical gates were used.

**Wire List**

U1 = GAL

U2 = SN74LS74

VCC🡪U1-28, U2-14

GND🡪U1-14, U2-7

X🡪 U1-4 (input)

U1-16🡪A (output)

U1-26🡪B (output)

U1-2🡪U2-5 (Q0)

U1-3🡪U2-9 (Q1)

CLK🡪U2-3, U2-11

U2-3🡪C (output) //CLK output - to display the clock interval

It was finally time to assemble the circuit. The sample binary “10110010101001010” was be inputted, but we couldn’t configure the GAL chip correctly. We never found the matching chip in the software last lab, so no one was able to make the GAL chip work again. We tried many variations, but none of them worked correctly and time ran out.